

# M95512RDW6TP

# Componente Almacén 1

## Description

The M95512 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 65536 x 8 bits, accessed through the SPI bus.

The M95512-W can operate with a supply voltage from 2.5 V to 5.5 V, the M95512-R can operate with a supply voltage from 1.8 V to 5.5 V and the M95512-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

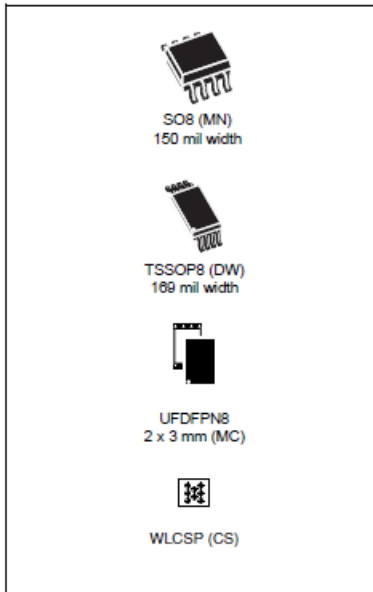
The M95512-D offers an additional page, named the Identification Page (128 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.



## M95512-W M95512-R M95512-DF

512-Kbit serial SPI bus EEPROM

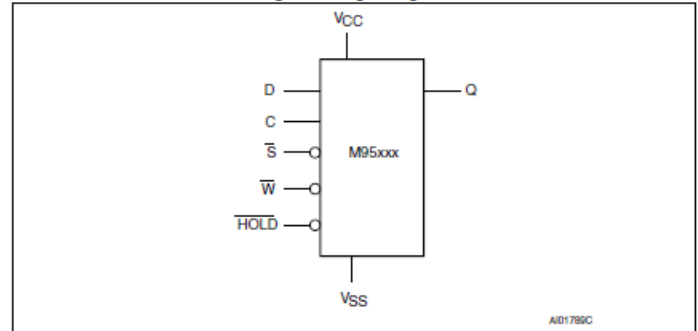
Datasheet - production data



### Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 512 Kb (64 Kbytes) of EEPROM
  - Page size: 128 bytes
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Additional Write lockable page (Identification page)
- Write Protect: quarter, half or whole memory array
- High-speed clock: 16 MHz
- Single supply voltage:
  - 2.5 V to 5.5 V for M95512-W
  - 1.8 V to 5.5 V for M95512-R
  - 1.7 V to 5.5 V for M95512-DF
- Operating temperature range: from -40°C up to +85°C
- Enhanced ESD protection
- More than 4 million Write cycles
- More than 200-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)

Figure 1. Logic diagram

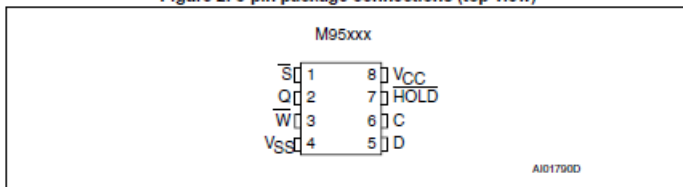


The SPI bus signals are C, D and Q, as shown in Figure 1 and Table 1. The device is selected when Chip Select ( $\bar{S}$ ) is driven low. Communications with the device can be interrupted when the HOLD is driven low.

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
$\bar{S}$	Chip Select	Input
W	Write Protect	Input
HOLD	Hold	Input
V <sub>CC</sub>	Supply voltage	-
V <sub>SS</sub>	Ground	-

Figure 2. 8-pin package connections (top view)



1. See Section 10: Package mechanical data for package dimensions, and how to identify pin-1.

Figure 3. WLCSP connections for M95512-DFCS6TP/K

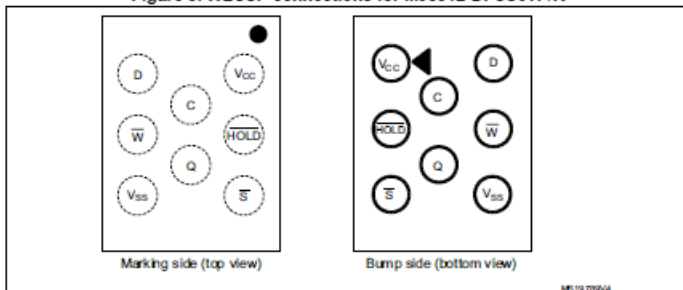
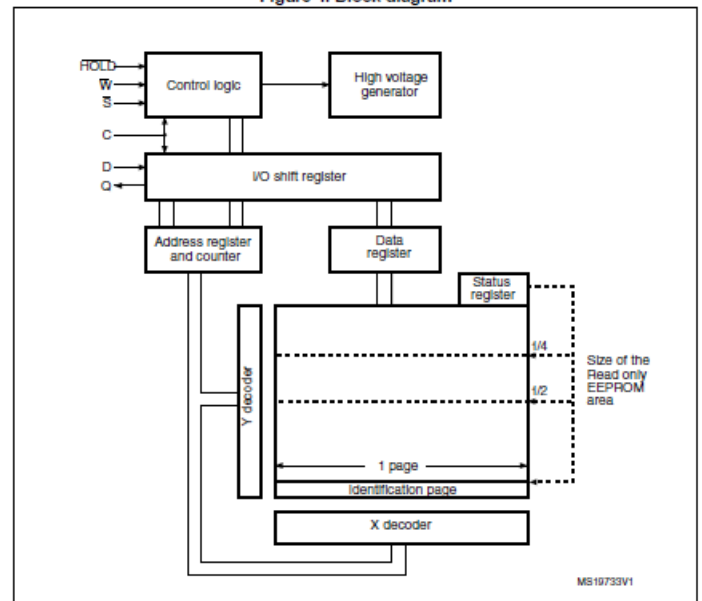


Figure 4. Block diagram



## Signal description

During all operations,  $V_{CC}$  must be held stable and within the specified valid range:  $V_{CC}(\text{min})$  to  $V_{CC}(\text{max})$ .

All of the input and output signals must be held high or low (according to voltages of  $V_{IH}$ ,  $V_{OH}$ ,  $V_{IL}$  or  $V_{OL}$ , as specified in [Section 9: DC and AC parameters](#)). These signals are described next.

### Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

### Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

### Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).

### Chip Select ( $\overline{S}$ )

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby Power mode, unless an internal Write cycle is in progress. Driving Chip Select ( $\overline{S}$ ) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ( $\overline{S}$ ) is required prior to the start of any instruction.

### Hold ( $\overline{HOLD}$ )

The Hold ( $\overline{HOLD}$ ) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ( $\overline{S}$ ) driven low.

### Write Protect ( $\overline{W}$ )

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all Write instructions.

### $V_{CC}$ supply voltage

$V_{CC}$  is the supply voltage.

### $V_{SS}$ ground

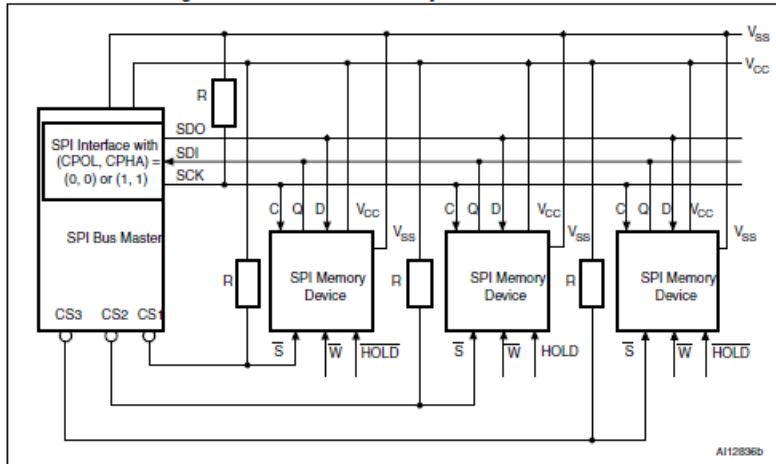
$V_{SS}$  is the reference for all signals, including the  $V_{CC}$  supply voltage.

## 4 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ( $\bar{S}$ ) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 5. Bus master and memory devices on the SPI bus



1. The Write Protect ( $\bar{W}$ ) and Hold ( $\overline{\text{HOLD}}$ ) signals should be driven, high or low as appropriate.

Figure 5 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (represented in Figure 5) ensures that a device is not selected if the Bus Master leaves the  $\bar{S}$  line in the high impedance state.

In applications where the Bus Master may leave all SPI bus lines in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the  $\bar{S}$  line is pulled high): this ensures that  $\bar{S}$  and C do not become high at the same time, and so, that the  $t_{\text{HCH}}$  requirement is met. The typical value of R is 100 k $\Omega$ .

### Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

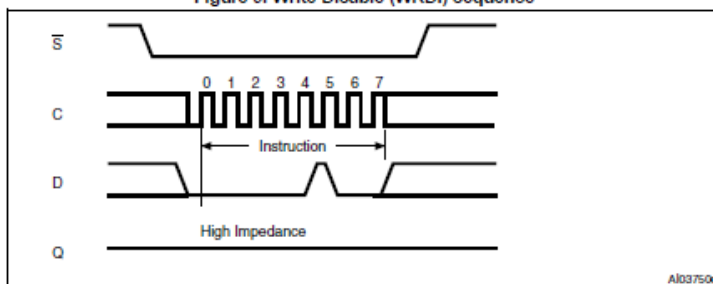
As shown in Figure 9, to send this instruction to the device, Chip Select ( $\bar{S}$ ) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for the device to be deselected, by Chip Select ( $\bar{S}$ ) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 9. Write Disable (WRDI) sequence



### SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

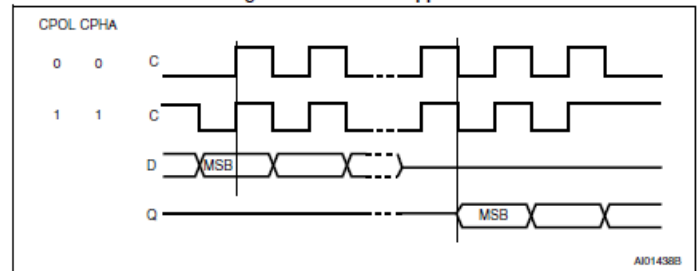
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 6, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 6. SPI modes supported



### Write Status Register (WRSR)

The Write Status Register (WRSR) instruction is used to write new values to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ( $\bar{S}$ ) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ( $\bar{S}$ ) driven high. Chip Select ( $\bar{S}$ ) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in Figure 11.

Figure 11. Write Status Register (WRSR) sequence

